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(54) Method for VIA etching in organo-silica-glass

(57) According to one embodiment of the invention, a method for via etching in a dielectric material includes providing a wafer (200) having a substrate (202), an etch stop layer (210) disposed outwardly from the substrate, an Organo-Silica-Glass layer (212) disposed outwardly from the etch stop layer (210), and a photoresist layer (216) disposed outwardly from the Organo-Silica-Glass layer (212), and positioning the wafer (200) within a process chamber (114). The method further includes in-

roducing a first source gas mixture (110) into the process chamber (114) to etch a first portion of the Organo-Silica-Glass layer (212) utilizing the first source gas mixture (110), and introducing a second source gas mixture (110) into the process chamber (114) to etch, for a predetermined time period, a second portion of the Organo-Silica-Glass layer (212) down to the etch stop layer (210). The second source gas mixture (110) includes a fluorocarbon, a noble gas, carbon monoxide, and nitrogen.

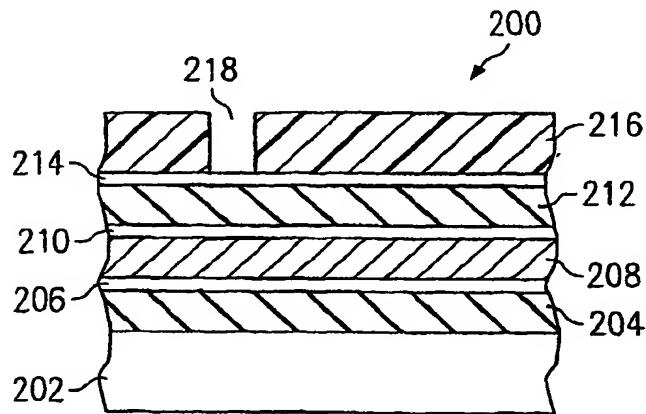


FIG. 2A

Description**TECHNICAL FIELD OF THE INVENTION**

[0001] This invention relates generally to the field of semiconductor devices and, more specifically, to a method for via etching in Organo-Silica-Glass ("OSG").

BACKGROUND OF THE INVENTION

[0002] Electronic equipment, such as televisions, telephones, radios, and computers, are often constructed using semiconductor components, such as integrated circuits and microprocessors. In an effort to ramp microprocessor speed semiconductor component manufacturers have become increasingly concerned with the RC time delay of interconnects. Some of the most publicized changes involve changes from aluminum to copper interconnects, but this alone does not meet speed requirements. A more effective approach is to simultaneously reduce line resistance and line capacitance. This is accomplished through the introduction of low-k dielectric materials (i.e., dielectric materials having a low dielectric constant and a high resistance) to take the place of high-k silica dielectrics. In addition, the associated etch stop and barrier layers, used to both protect the copper from exposure during processing and to provide an etch stop layer for the via etches, may also be switched from high dielectric to low dielectric materials. For example, the industry has been moving from silicon nitride etch stop layers to silicon carbide etch stop layers.

[0003] Because of the recent use of these low-k dielectric materials, the etching of the vias must be performed with great care. Accordingly, the etch stop layer may be etched all the way down to the underlying copper layer before the etch process is finished. This may result in some of the copper diffusing into the low-k dielectric layer leading to shorts in the interconnect layers, which may be devastating to the microprocessor.

SUMMARY OF THE INVENTION

[0004] According to one embodiment of the invention, a method for via etching in a dielectric material includes providing a wafer having a substrate, an etch stop layer disposed outwardly from the substrate, an Organo-Silica-Glass layer disposed outwardly from the etch stop layer, and a photoresist layer disposed outwardly from the Organo-Silica-Glass layer, and positioning the wafer within a process chamber. The method further includes introducing a first source gas mixture into the process chamber to etch a first portion of the Organo-Silica-Glass layer utilizing the first source gas mixture, and introducing a second source gas mixture into the process chamber to etch, for a predetermined time period, a second portion of the Organo-Silica-Glass layer down to the etch stop layer. The second source gas mixture includes a fluorocarbon, a noble gas, carbon monoxide, and ni-

trogen.

[0005] Embodiments of the invention provide a number of technical advantages. Embodiments of the invention may include all, some, or none of these advantages. By using certain combinations of reactive gases in a plasma etching process, a very high selectivity over the etch stop layer may be obtained, while still maintaining a high etch rate and proper via profile formation. This high selectivity guarantees a higher clearing of all vias, as well as substantially reducing the risk of copper diffusion into an OSG layer. Thinner etch stop layers may also be obtained, which helps to reduce line resistance and line capacitance, thereby decreasing the RC time delay of interconnects.

[0006] Other technical advantages are readily apparent to one skilled in the art from the following figures, descriptions, and claims.

BRIEF DESCRIPTION OF THE DRAWINGS

[0007] For a more complete understanding of the invention, and for further features and advantages, reference is now made to the following description, taken in conjunction with the accompanying drawings, in which:

25 FIGURE 1 is a schematic diagram of a plasma etching system used to etch one or more wafers in accordance with one embodiment of the present invention;

30 FIGURES 2A through 2D are partial elevation views of a wafer illustrating a method for via etching in an Organo-Silica-Glass layer according to one embodiment of the present invention; and

35 FIGURE 3 is a partial elevation view of the wafer of FIGURES 2A through 2D illustrating two copper layers interconnected with a copper plug.

DETAILED DESCRIPTION OF EXAMPLE EMBODIMENTS OF THE INVENTION

40 **[0008]** Example embodiments of the present invention and their advantages are best understood by referring now to FIGURES 1 through 3 of the drawings, in which like numerals refer to like parts.

45 **[0009]** FIGURE 1 is a schematic diagram of a plasma etching system 100 used to etch one or more wafers 200 in accordance with one embodiment of the present invention. Plasma etching system 100 may include a source gas supply system 102, a reactor system 104, and a gas exhaust system 106. Generally, source gas supply system 102 operates to supply a source gas mixture 110 to reactor system 104, reactor system 104 utilizes source gas mixture 110 to form a reactive plasma 108 that is used to etch wafer 200, and gas exhaust system 106 removes an exhaust gas 112. The chemistry of source gas mixture 110 may be varied to selectively etch the various materials comprising wafer 200. The composition of exhaust gas 112 is indicative of the materials

being etched or indicative of when source gas mixture 110 has reached steady state condition. A control system (not explicitly shown) may control the operation of each component in plasma etching system 100 to etch wafer 200 in a desired manner. Plasma etching system 100 may comprise other suitable components and systems without departing from the scope of the present invention.

[0010] Source gas supply system 102 includes individual source gases, such as oxygen, nitrogen, fluorocarbon, carbon monoxide, argon, xenon, and other suitable gases. A source gas controller in source gas supply system 102 receives the individual source gases and mixes the gases to form source gas mixture 110 that is supplied to reactor system 104. Source gas mixture 110 has an associated chemistry that is determined by the individual source gases and their quantity used in source gas mixture 110. As discussed in greater detail below, the chemistry of source gas mixture 110 determines the selectivity of reactive plasma 108 to various materials. Source gas supply system 102 may comprise other suitable devices and systems without departing from the scope of the present invention.

[0011] Reactor system 104 includes a plasma chamber 114 that includes an upper electrode 116, a rotatable base 118, and a lower electrode 120 coupled to base 118. A power supply system 122 is coupled to upper electrode 116 and lower electrode 120. Wafer 200, to be etched, may be generally rotated by base 118 during the etching process. Electrodes 116 and 120, when turned on, operate to ionize source gas mixture 110 flowing through plasma chamber 114 and ignite source gas mixture 110 to form reactive plasma 108. Reactor system 104 may comprise other suitable devices or systems without departing from the scope of the present invention.

[0012] Gas exhaust system 106 may comprise such devices as an endpoint detector and a pumping system. The pumping system operates to maintain the pressure within plasma chamber 114 at acceptable vacuum pressures. The endpoint detector operates to determine the composition of exhaust gas 112. The endpoint detector may sense which materials within wafer 200 are being consumed during the etching process. Gas exhaust system 106 may comprise other suitable devices or systems without departing from the scope of the present invention.

[0013] In the general operation of plasma etching system 100, wafer 200 is positioned in plasma chamber 114. Plasma chamber 114 is then vacuum sealed and plasma etching system 100 is engaged. A control system turns on a pumping system in gas exhaust system 106 and source gas supply system 102. Source gas mixture 110 may initially flow only a purge gas for a specified time to purge plasma chamber 114. After purging plasma chamber 114, source gas mixture 110 is then varied to a predetermined etching chemistry. When the proper etching chemistry has stabilized, power supply system

122 is turned on. Power supply system 122 provides RF power to electrodes 116 and 120 such that source gas mixture 110 is ionized and ignited to form reactive plasma 108. Reactive plasma 108 is directed at wafer 200.

5 Reactive plasma 108 anisotropically etches the exposed surfaces of wafer 200. When reactive plasma 108 has etched through the applicable materials and starts etching through another material an endpoint detector in gas exhaust system 106 senses the change in material being etched. Depending upon the etching processes to be performed, a control system could turn off power supply system 122 in response to the change in material being etched, or the control system may vary the chemistry of source gas mixture 110 and thereby vary 10 the composition of reactive plasma 108 to anisotropically etch through a new material.

[0014] According to the teachings of the present invention, source gas mixture 110 includes one or more predetermined chemistries for etching vias in Organosilica-Glass ("OSG"), such that a high selectivity is obtained while maintaining other important etching criteria, such as etch rate and uniformity. One method for via etching in a dielectric material is illustrated in FIGURES 2A through 2D.

20 [0015] FIGURES 2A through 2D are partial elevation views of wafer 200 illustrating a method for via etching in OSG according to one embodiment of the present invention. Wafer 200 may include a substrate 202, a dielectric layer 204, a buffer layer 206, a metal layer 208, an etch stop layer 210, and OSG layer 212, a buffer layer 214, and a photoresist layer 216. Wafer 200 may have less layers, more layers, or layers formed from different materials than described herein. Wafer 200 is only example of a semiconductor wafer having various layers.

30 [0016] Substrate 200 may be formed from any suitable material used in semiconductor chip fabrication, such as silicon or germanium. Although not illustrated in FIGURE 2A, substrate 202 has any of various microelectronic devices formed therein, such as transistors, diodes, resistors, and capacitors. Substrate 200 may be formed with any suitable thickness.

35 [0017] Dielectric layer 204 comprises any suitable type of dielectric, such as oxide or nitride, and is formed using any suitable growth and/or deposition technique used in semiconductor processing. Dielectric layer 204 is an optional layer, and in one embodiment, dielectric layer 204 electrically insulates the microelectronic devices formed in substrate 202 from metal layer 208. Dielectric layer 204 may also be used in forming a gate stack outwardly from substrate 202. Dielectric layer 204 may be formed with any suitable thickness.

40 [0018] Buffer layer 206 comprises any suitable type of dielectric, such as silicon nitride or silicon carbide, and is formed using any suitable growth and/or deposition technique used in semiconductor processing. Buffer layer 206, in one embodiment, is used as an etch stop for the etching of metal layer 208. Buffer layer 206 may be formed with any suitable thickness, but is typically

between 300 and 1000 angstroms.

[0019] Metal layer 208 is formed from any suitable conductive material, such as copper or aluminum, and is formed using any suitable growth and/or deposition technique used in semiconductor processing. Metal layer 208 operates, in whole or in part, as a conductive path from one or more microelectronic devices formed in substrate 202 to other microelectronic devices formed in substrate 202. In one embodiment, metal layer 208 is formed with a thickness of approximately 5000 angstroms; however, other suitable thicknesses may be used.

[0020] Etch stop layer 210 is formed from any suitable type of dielectric, such as silicon carbide or silicon nitride, and is formed using any suitable growth and/or deposition technique using semiconductor processing. As discussed in greater detail below, etch stop layer 210 is used in the etching of OSG layer 212 to prevent over-etching, such that any metal from metal layer 208 will not diffuse into OSG layer 212 when etching a via. Etch stop layer 210 is typically formed with a thickness of approximately 300 angstroms to 1000 angstroms; however, other suitable thicknesses may be used. In one particular embodiment, etch stop layer 210 is formed with a thickness of no more than approximately 500 angstroms.

[0021] OSG layer 212, in one embodiment, is formed from Organo-Silica-Glass ("OSG"); however, other suitable organic dielectric materials may be used for OSG layer 212. Typically, the type of dielectric material used for OSG layer 212 is a high-resistance low-K dielectric material. OSG layer 212 is preferably made of a low-K dielectric material because semiconductor manufacturers desire to reduce line resistance and line capacitance to speed up, for example, processor speed of a microprocessor. In one embodiment, OSG layer 212 is formed with a thickness of approximately 8000 angstroms to 12000 angstroms; however, other suitable thicknesses may be used.

[0022] Buffer layer 214 is similar to buffer layer 206 and that is formed from any suitable dielectric material, such as silicon carbide or silicon nitride, and is formed using any suitable growth and/or deposition technique used in semiconductor processing. Again, buffer layer 214 is used as an etch stop layer for the etching of a metal layer that is disposed outwardly from buffer layer 214 (not shown). Buffer layer 214 is typically formed with a thickness of approximately 300 angstroms to 1000 angstroms; however, other suitable thicknesses may be used.

[0023] Photoresist layer 216 is formed by conventional photolithography techniques. Any suitable photoresist material may be used to form photoresist layer 216. Photoresist layer 216 includes one or more windows 218, which is formed using any suitable photolithographic techniques known in the art of semiconductor processing. Window 218 is where a via is to be formed in wafer 200, as discussed more fully below.

[0024] Formation of a via in wafer 200 is described in detail below in conjunction with FIGURES 2B through 2D with additional reference to FIGURE 1. Although not illustrated in FIGURES 2B through 2D, the below description refers to steps that occur when wafer 200 is positioned in plasma chamber 114 (FIGURE 1). However, the etching processes may take place in different processing chambers using one or more various etching techniques.

[0025] FIGURE 2B illustrates an etching of a portion of buffer layer 214 and a first portion 220 of OSG layer 212. This etching process may be performed using any suitable etching process; however, in one embodiment, a low-selectivity, low-polymerizing, main etch is performed using reactive plasma 108 formed from an ionized gas mixture 110 that includes a fluorocarbon and nitrogen. Preferably, a majority of OSG layer 212 is etched away using this relatively fast etching process. For example, if OSG layer 212 is approximately 8000 angstroms thick, then the etching depth of first portion 220 is approximately 7000 angstroms. However, OSG layer 212 may be etched down to any suitable depths using any suitable etching techniques.

[0026] FIGURE 2C illustrates the etching of a second portion 222 of OSG layer 212 down to etch stop layer 210 utilizing reactive plasma 108 that is formed from an ionized source gas mixture 110 that is different from the ionized source gas mixture 110 that is used for the main etch as described above in FIGURE 2B. The reason source gas mixture 110 is different for the two processes shown in FIGURES 2B and 2C is because the etching of the via is getting closer to the surface of metal layer 208. Any over-etching should be avoided at this point in the via etching because diffusion of metal from metal layer 208 into OSG layer 212 may be devastating to one or more microelectronic devices fabricated in wafer 200. The etching of second portion 222 is performed for a predetermined time period, such as 30 to 90 seconds. However, other suitable time periods may be utilized.

[0027] Source gas mixture 110 used to form reactive plasma 108, in one embodiment, comprises a fluorocarbon, a noble gas, carbon monoxide, and nitrogen. In other embodiments, oxygen is also added to source gas mixture 110. Preferably, a volumetric flow rate of the fluorocarbon, the noble gas, the carbon monoxide, and the nitrogen is such that a selectivity of the material in OSG layer 212 to the material in etch stop layer 210 is no less than approximately 15:1. As examples, a volumetric flow rate of the fluorocarbon may be between 2 and 20 sccm, a volumetric flow rate of a noble gas is between 100 and 400 sccm, a volumetric flow rate of the carbon monoxide is between 50 and 200 sccm, a volumetric flow rate of nitrogen is between 90 and 250 sccm, and a volumetric flow rate of the oxygen, if present, is less than approximately 10 sccm. In one embodiment where oxygen is a part of source gas mixture 110, a carbon monoxide:oxygen volumetric flow rate ratio is approximately 20:1.

[0028] Because OSG contains a CH₃ organic group, an increase in polymerization is obtained, which increases the amount of polymer formed through the etch process. This may result in etch stop if no nitrogen is used. Therefore, a relatively high volumetric flow rate of nitrogen is required to attack the CH₃ organic group of OSG so that etch stop may be prevented. As described above, in one embodiment, a sufficient volumetric flow rate of nitrogen is between 90 and 250 sccm. A more advantageous volumetric flow rate of nitrogen is between 95 and 180 sccm, and a particular volumetric flow rate of nitrogen that has shown to give excellent results in attacking the CH₃ organic group of OSG is between 100 and 110 sccm. In another particular embodiment, a volumetric flow rate of nitrogen is sufficient to remove an ethyl group of the OSG at a rate that is at least as fast as the rate of removal of the silica group of the OSG.

[0029] Depending upon the materials being etched and the process and quality parameters, the gases that make up source gas mixture 110 for etching second portion 222 are adjusted to obtain the desired results. An important result is that all vias are cleared while avoiding any over-etching into the metal of metal layer 208 to avoid any diffusion of the metal into OSG layer 212; this is why high selectivity is desired. The achievement of high selectivity allows etch stop layer 210 to be thinner, which improves the device or devices fabricated in wafer 200 by reducing the RC time delay of the interconnects. To complete the formation of the via, etch stop layer 210 must be removed. This is illustrated in FIGURE 2D.

[0030] FIGURE 2D illustrates the removal of a portion of etch stop layer 210 to complete via formation. Any suitable well known etching techniques may be used to remove the portion of etch stop layer 210. One such well known technique is referred to as an e-stop etch, in which sidewalls 224 are formed using a suitable passivation technique before the portion of etch stop layer 210 is removed with, for example, an argon bombardment 226. After removing the portion of etch stop layer 210, wafer 200 is cleaned using any suitable cleaning techniques well known in the art of semiconductor processing. Thereafter, metal layer 208 may be interconnected with a second metal layer 228 and a plug 230 as illustrated in FIGURE 3.

[0031] FIGURE 3 illustrates the interconnection of metal layer 208 with second metal layer 228 using plug 230. Second metal layer 228 and plug 230 are preferably formed from the same material as metal layer 210 and is formed using any suitable growth and/or deposition techniques used in semiconductor processing. Although not illustrated, further processing may be performed on wafer 200 outwardly from second metal layer 228, such as the addition of other metal layers so that other microelectronic devices formed in substrate may be interconnected.

[0032] Although embodiments of the invention and their advantages are described in detail, a person skilled in the art could make various alterations, additions, and

omissions without departing from the spirit and scope of the present invention as defined by the appended claims.

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Claims

1. A method for via etching in a dielectric material, comprising:

providing a wafer having a substrate, an etch stop layer disposed outwardly from the substrate, an Organo-Silica-Glass layer disposed outwardly from the etch stop layer, and a photoresist layer disposed outwardly from the Organo-Silica-Glass layer; positioning the wafer within a process chamber; introducing a first source gas mixture into the process chamber; etching a first portion of the Organo-Silica-Glass layer utilizing the first source gas mixture; introducing a second source gas mixture into the process chamber, the second source gas mixture comprising a fluorocarbon, a noble gas, carbon monoxide, and nitrogen; and etching, for a predetermined time period, a second portion of the Organo-Silica-Glass layer down to the etch stop layer utilizing the second source gas mixture.

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2. The method of Claim 1, wherein providing the wafer comprises providing a wafer having an etch stop layer formed from a material selected from the group consisting of silicon carbide and silicon nitride, the etch stop layer being formed with a thickness of no more than approximately 500 angstroms.

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3. The method of Claim 2, wherein a volumetric flow rate of the fluorocarbon, the noble gas, the carbon monoxide, and the nitrogen is such that a selectivity of the Organo-Silica-Glass to the etch stop layer is no less than approximately 15-to-1.

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4. The method of Claim 1 or Claim 2, wherein introducing the second source gas mixture into the process chamber comprises introducing a second source gas mixture into the process chamber, the second source gas mixture comprising a fluorocarbon, a noble gas, carbon monoxide, nitrogen, and oxygen.

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5. The method of any preceding claim, wherein a volumetric flow rate of the fluorocarbon is between 2 and 20 sccm.

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6. The method of any preceding claim, wherein a volumetric flow rate of the noble gas is between 100

- and 400 sccm.
7. The method of any preceding claim, wherein a volumetric flow rate of the carbon monoxide is between 50 and 200 sccm.
8. The method of any of claims 4 to 7, wherein the volumetric flow rate of the nitrogen is between 90 and 250 sccm.
9. The method of any of claims 4 to 9, wherein a volumetric flow rate of the oxygen is less than 10 sccm.
10. A method for via etching in a dielectric material, comprising:
- providing a wafer having a substrate, an etch stop layer disposed outwardly from the substrate, an Organo-Silica-Glass layer disposed outwardly from the etch stop layer, and a photoresist layer disposed outwardly from the Organo-Silica-Glass layer;
- positioning the wafer within a process chamber;
- introducing a first source gas mixture into the process chamber;
- etching a first portion of the Organo-Silica-Glass layer utilizing the first source gas mixture;
- introducing a second source gas mixture into the process chamber, the second source gas mixture comprising a fluorocarbon, a noble gas, carbon monoxide, nitrogen, and oxygen, a volumetric flow rate of the nitrogen being between 90 and 250 sccm for attacking an ethyl group of the Organo-Silica-Glass;
- etching, for a predetermined time period, a second portion of the Organo-Silica-Glass layer down to the etch stop layer utilizing the second source gas mixture, wherein a volumetric flow rate of the fluorocarbon, the noble gas, the carbon monoxide, the nitrogen, and the oxygen is such that a selectivity of the Organo-Silica-Glass to Silicon Carbide is no less than approximately 15-to-1;
- removing the etch stop layer; and
- cleaning the wafer.
11. The method of Claim 10, wherein providing the wafer comprises providing a wafer having an etch stop layer formed from a material selected from the group consisting of silicon carbide and silicon nitride, the etch stop layer being formed with a thickness of no more than approximately 500 angstroms.
12. The method of Claim 10 or Claim 11, wherein a volumetric flow rate of the fluorocarbon is between 2 and 20 sccm, a volumetric flow rate of the noble gas is between 100 and 400 sccm, a volumetric flow rate of the carbon monoxide is between 50 and 200 sccm, and a volumetric flow rate of the oxygen is less than 10 sccm.
- 5 13. The method of Claim 10, Claim 11 or Claim 12, wherein the carbon monoxide:oxygen volumetric flow rate ratio is approximately 20:1.
- 10 14. The method of any of claims 10 to 13, wherein etching, for the predetermined time period, the second portion of the Organo-Silica-Glass layer down to the etch stop layer utilizing the second source gas mixture comprises etching for a time period between 30 and 90 seconds.
- 15 15. The method of any of claim 10 to 14, wherein the volumetric flow rate of the nitrogen is between 100 and 110 sccm.
- 20 16. A method for via etching in a dielectric material, comprising:
- providing a wafer having a substrate, a silicon carbide layer having a thickness of no more than approximately 500 angstroms disposed outwardly from the substrate, an Organo-Silica-Glass layer disposed outwardly from the silicon carbide layer, and a photoresist layer disposed outwardly from the Organo-Silica-Glass layer;
- positioning the wafer within a process chamber;
- introducing a first source gas mixture into the process chamber;
- etching a first portion of the Organo-Silica-Glass layer utilizing the first source gas mixture;
- introducing a second source gas mixture into the process chamber, the second source gas mixture comprising a fluorocarbon, argon, carbon monoxide, nitrogen, and oxygen;
- etching, for a time period between approximately thirty and ninety seconds, a second portion of the Organo-Silica-Glass layer down to the silicon carbide layer utilizing the second source gas mixture, the second source gas mixture having a volumetric flow rate of the fluorocarbon of between 2 and 20 sccm, a volumetric flow rate of the argon of between 100 and 400 sccm, a volumetric flow rate of the carbon monoxide of between 50 and 200 sccm, and a volumetric flow rate of the oxygen is less than 10 sccm, and a volumetric flow rate of the nitrogen that is sufficient to remove an ethyl group of the Organo-Silica-Glass at a rate that is at least as fast as the rate of removal of a silica group of the Organo-Silica-Glass;
- etching the etch stop layer; and
- cleaning the wafer.

17. The method of Claim 16, wherein the carbon monoxide:oxygen volumetric flow rate ratio is approximately 20:1.
18. The method of Claim 16, wherein the volumetric flow rate of the nitrogen is between 90 and 250 sc-
cm. 5
19. The method of Claim 16, wherein the volumetric flow rate of the nitrogen is between 95 to 180 sccm. 10
20. The method of Claim 16, wherein the volumetric flow rate of the nitrogen is between 100 to 110 sccm.

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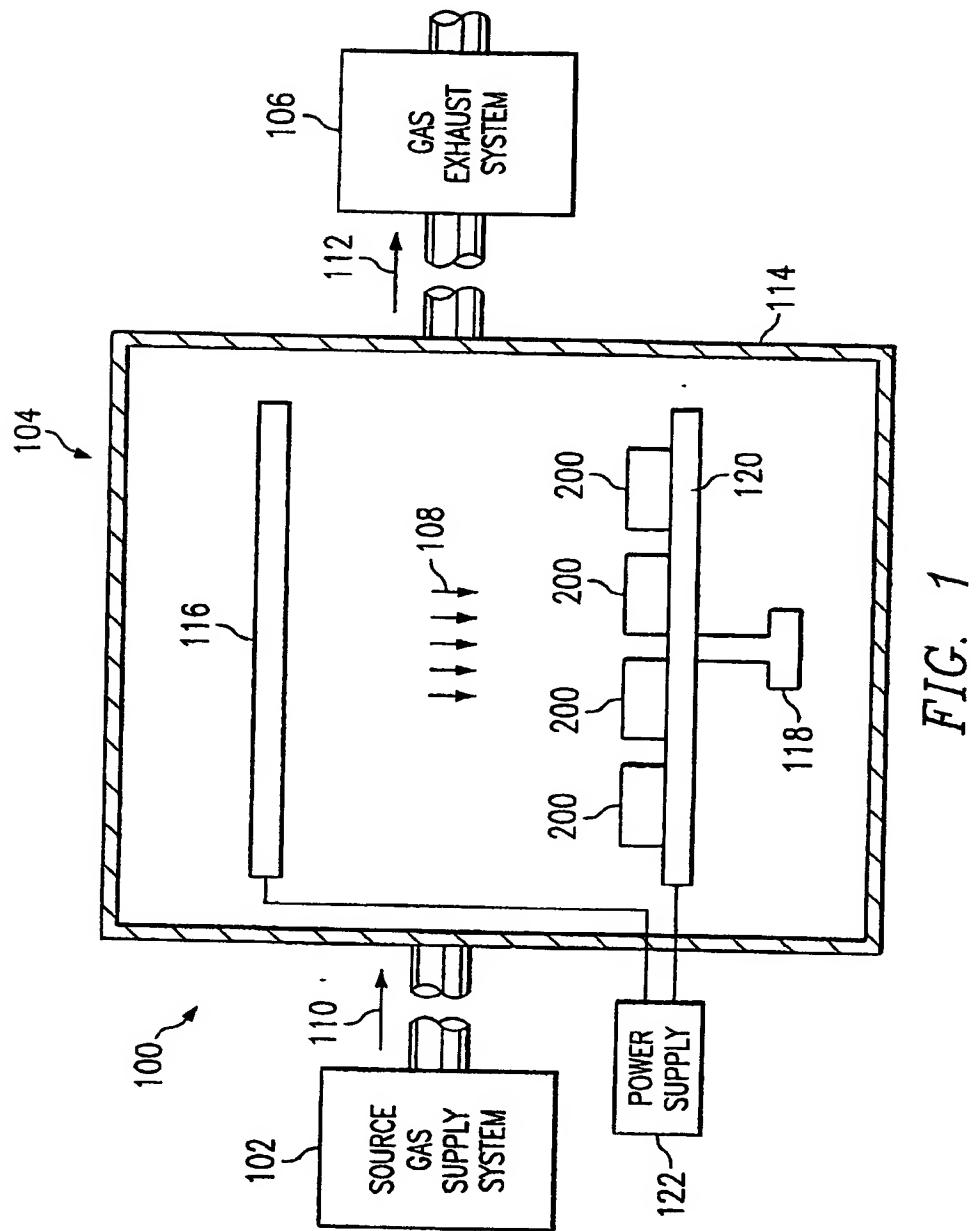


FIG. 1

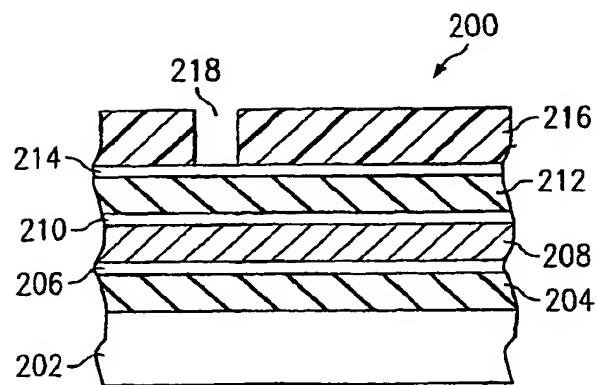


FIG. 2A

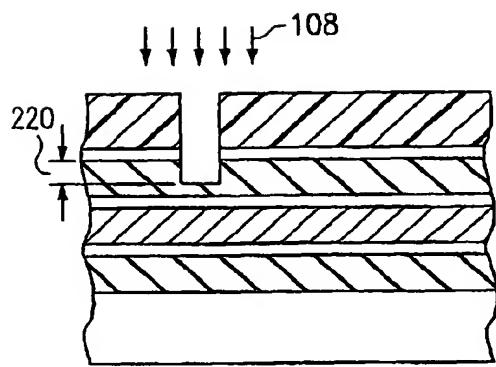


FIG. 2B

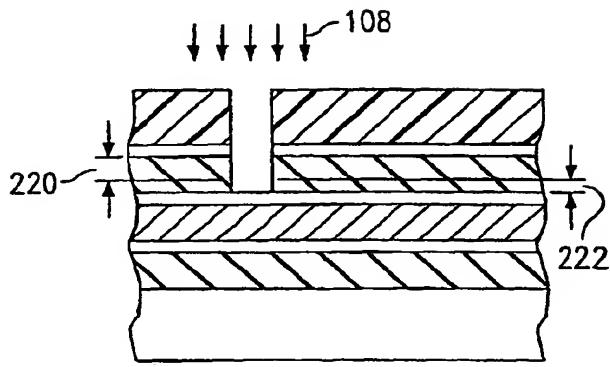


FIG. 2C

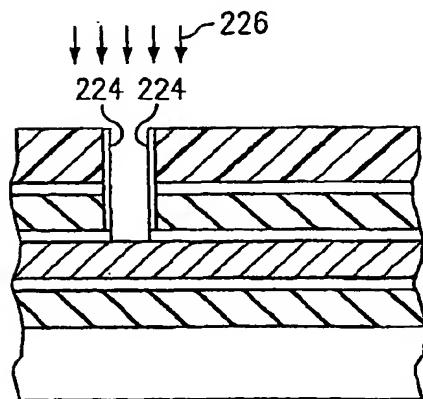


FIG. 2D

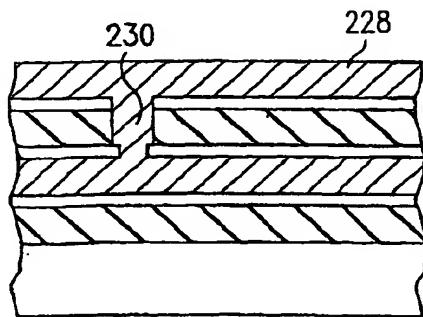


FIG. 3

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(54) Method for VIA etching in organo-silica-glass

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roducing a first source gas mixture (110) into the process chamber (114) to etch a first portion of the Organo-Silica-Glass layer (212) utilizing the first source gas mixture (110), and introducing a second source gas mixture (110) into the process chamber (114) to etch, for a pre-determined time period, a second portion of the Organo-Silica-Glass layer (212) down to the etch stop layer (210). The second source gas mixture (110) includes a fluorocarbon, a noble gas, carbon monoxide, and nitrogen.

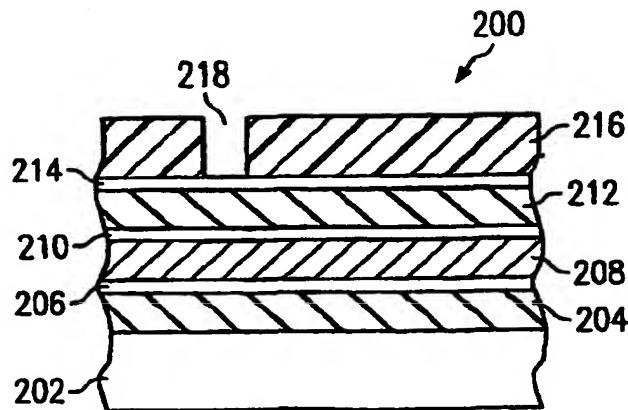


FIG. 2A



European Patent
Office

EUROPEAN SEARCH REPORT

Application Number

EP 02 02 1964

DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.7)
X	EP 1 085 563 A (MOTOROLA INC) 21 March 2001 (2001-03-21) * the whole document *	1-3, 5-8	H01L21/311
X	PATENT ABSTRACTS OF JAPAN vol. 2000, no. 25, 12 April 2001 (2001-04-12) -& JP 2001 210627 A (MATSUSHITA ELECTRIC IND CO LTD), 3 August 2001 (2001-08-03) * abstract * * paragraph '0062! - paragraph '0065! * * paragraph '0104! - paragraph '0116! * * paragraph '0151! - paragraph '0167! * * paragraph '0188! - paragraph '0203! *	10, 16 1	
X	US 6 083 844 A (BUI-LE GIAO QUYNH ET AL) 4 July 2000 (2000-07-04) * column 5, line 40 - column 7, line 10 * * column 3, line 12 - line 16 *	1, 5-7	
X	US 6 143 665 A (HSIEH CHI-KUO) 7 November 2000 (2000-11-07) * column 5, line 53 - column 6, line 20 *	1, 5, 7	TECHNICAL FIELDS SEARCHED (Int.Cl.7) H01L
X	US 6 211 063 B1 (LIU JEN-CHENG ET AL) 3 April 2001 (2001-04-03) * column 5 *	1	
A	US 6 168 726 B1 (DING JIAN ET AL) 2 January 2001 (2001-01-02) * column 12, line 66 - column 13, line 6 *	1-20	
A	EP 1 059 664 A (APPLIED MATERIALS INC) 13 December 2000 (2000-12-13) * paragraph '0071! - paragraph '0076! *	1-20 -/-	
The present search report has been drawn up for all claims			
Place of search THE HAGUE		Date of completion of the search 28 April 2004	Examiner Szarowski, A
CATEGORY OF CITED DOCUMENTS			
X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document			
T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons & : member of the same patent family, corresponding document			

European Patent
Office

EUROPEAN SEARCH REPORT

Application Number
EP 02 02 1964

DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.7)
A	US 2001/005634 A1 (KAIJIWARA SEIJI) 28 June 2001 (2001-06-28) * paragraphs '0126!, '0153!; claims 1,2 *	1-20	
P,X	GB 2 368 457 A (IBM) 1 May 2002 (2002-05-01) * the whole document *	1-20	
P,X	PATENT ABSTRACTS OF JAPAN vol. 2003, no. 01, 14 January 2003 (2003-01-14) -& JP 2002 270586 A (TOKYO ELECTRON LTD), 20 September 2002 (2002-09-20) * abstract * * paragraphs '0002!, '0003! *	1	
E	US 2003/211750 A1 (KIM YUNSANG ET AL) 13 November 2003 (2003-11-13) * paragraph '0061! - paragraph '0075! *	1-3,6,8	
E	US 2002/164877 A1 (SCHINELLA RICHARD ET AL) 7 November 2002 (2002-11-07) * paragraphs '0025!, '0026!, '0034! *	1,4	TECHNICAL FIELDS SEARCHED (Int.Cl.7)
E	US 2003/235993 A1 (KOMATSU TAKEHIKO ET AL) 25 December 2003 (2003-12-25) * paragraphs '0032!, '0041!, '0048! *	1,4	
The present search report has been drawn up for all claims			
Place of search	Date of completion of the search	Examiner	
THE HAGUE	28 April 2004	Szarowski, A	
CATEGORY OF CITED DOCUMENTS		T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons & : member of the same patent family, corresponding document	
X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document			

ANNEX TO THE EUROPEAN SEARCH REPORT
ON EUROPEAN PATENT APPLICATION NO.

EP 02 02 1964

This annex lists the patent family members relating to the patent documents cited in the above-mentioned European search report. The members are as contained in the European Patent Office EDP file on The European Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

28-04-2004

Patent document cited in search report		Publication date		Patent family member(s)	Publication date
EP 1085563	A	21-03-2001	CN EP JP SG TW	1288253 A 1085563 A2 2001110792 A 93886 A1 455948 B	21-03-2001 21-03-2001 20-04-2001 21-01-2003 21-09-2001
JP 2001210627	A	03-08-2001	JP US	3400770 B2 2002061654 A1	28-04-2003 23-05-2002
US 6083844	A	04-07-2000	EP JP TW WO	1042796 A1 2001527288 T 446757 B 9933097 A1	11-10-2000 25-12-2001 21-07-2001 01-07-1999
US 6143665	A	07-11-2000	JP	11145114 A	28-05-1999
US 6211063	B1	03-04-2001		NONE	
US 6168726	B1	02-01-2001		NONE	
EP 1059664	A	13-12-2000	US EP JP TW US US	6340435 B1 1059664 A2 2001110789 A 473870 B 2002074309 A1 2002084257 A1	22-01-2002 13-12-2000 20-04-2001 21-01-2002 20-06-2002 04-07-2002
US 2001005634	A1	28-06-2001	JP TW	2001250817 A 486733 B	14-09-2001 11-05-2002
GB 2368457	A	01-05-2002	US JP TW	6720249 B1 2001351976 A 488026 B	13-04-2004 21-12-2001 21-05-2002
JP 2002270586	A	20-09-2002	EP WO TW	1367638 A1 02073674 A1 529105 B	03-12-2003 19-09-2002 21-04-2003
US 2003211750	A1	13-11-2003		NONE	
US 2002164877	A1	07-11-2002		NONE	
US 2003235993	A1	25-12-2003		NONE	